

10/8/03

PTO/SB/08A (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

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Substitute for form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	10/681,525
		Filing Date	10/8/2003
		First Named Inventor	Srinivasan, Varadarajan
		Art Unit	2827
		Examiner Name	G. M. Auduong
Sheet 1 of 1	Attorney Docket Number	NLMI.P133	

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
P		US- 5,042,011	08-20-1991	Casper et al.	3
		US- 5,280,205	01-18-1994	Green et al.	
		US- 5,627,785	05-06-1997	Gilliam et al.	
		US- 6,240,003	05-29-2001	McElroy	
		US- 6,320,777	11-20-2001	Lines et al.	
		US- 6,331,961	12-18-2001	Kengeri et al.	
		US- 6,400,593	06-04-2002	Lien et al.	
		US- 6,421,265	07-16-2002	Lien et al.	
		US- 6,430,073	08-06-2002	Batson et al.	
		US- 6,442,090	08-27-2002	Ahmed et al.	
Q		US- 6,483,733	11-19-2002	Lines et al.	
		US-			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

Examiner Signature	<i>G. M. Auduong</i>	Date Considered	4/05
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Sheet

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Filing Date	October 8, 2003
First Named Inventor	Srinivasan, Varadarajan
Art Unit	2827
Examiner Name	G. N. Auduong
Attorney Docket Number	NLMIP133

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**Examiner
Signature**

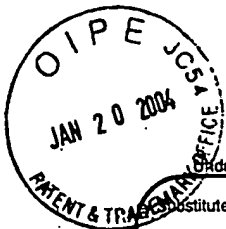
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Applicant Number	10/681,525
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First Named Inventor	Srinivasan, V.
Art Unit	2848 2827
Examiner Name	
Attorney Docket Number	NLM.P133

Sheet 1 of 1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
②		SAKURAI, T. et al., "A Low Power 46ns 256k bit CMOS Static RAM with Dynamic Double Word Line," IEEE Journal of Solid State Circuits, Vol. SC-19, No.5, October 1984, pp.578-585	
		SOOD, L. et al., "A Fast 8ki x 8 CMOS SRAM With Internal Power Down Design Techniques," IEEE Journal of Solid State Circuits, Vol. SC-20, No. 5, October 1985, pp.941-950	
		MIYAJI, F. et al., "A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads, IEEE Journal of Solid state Circuits," Vol. 24, No. 5, October 1989, pp.1213-1218	
		SASAKI, K. et al., "A 7-ns 140mW 1-Mb CMOS SRAM with Current Sense Amplifier," IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, pp. 1511-1518	
②		PRINCE, B., "Semiconductor Memories: A Handbook of Design, Manufacture and Application," 2nd Ed., John Wiley & Sons Ltd., West Sussex, England, 1995, pp. v-xvii, 401-404 and 4	

Examiner Signature	<i>Seo Seubang</i>	Date Considered	4/05
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